CLAIM AMENDMENTS

WHAT IS CLAIMED IS:

This listing of the claims will replace all prior versions, and listing, of claims in the application:

1. **(Currently Amended)** An integrated circuit ~~(1)~~ comprising function modules ~~(2)~~, wherein the function modules ~~(2)~~ comprise a central processing unit ~~(4), by means of which~~ **designed to process** data ~~can be processed~~ **and to execute** programs ~~can be executed~~, and a cache memory ~~(5)~~, wherein the function modules ~~(2)~~ comprise an encryption unit ~~(6) by means of which~~**designed to encrypt and decrypt** data ~~can be encrypted and decrypted~~ and the function modules ~~(2)~~ comprise a security sensor system ~~(9)~~ by means of which at least one operating parameter ~~(f, T, U)~~ of the integrated circuit ~~(1) can be~~**is** monitored, ~~characterized in that~~**wherein**, as operating parameters ~~(f, T, U)~~, the state of a protective layer ~~(20)~~ on the integrated circuit ~~(1)~~ is monitored.

2. **(Currently Amended)** The integrated circuit ~~(1) as claimed in~~**according to** claim 1, ~~characterized in that~~ **wherein** the function modules comprise a random-number generator ~~(80)~~.

3. **(Currently Amended)** **The integrated circuit according to claim 1, wherein** ~~The integrated circuit (1) as claimed in claim 1, characterized in that~~ the function modules ~~(2)~~

comprise a first memory ~~(7)~~ in which cryptological keys ~~(18)~~ are stored.

4. **(Currently Amended)** **The integrated circuit according to claim 3, wherein** ~~**The integrated circuit (1) as claimed in claim 2 and 3, characterized in that**~~ cryptological keys ~~(18)~~ which are stored in the first memory ~~(7)~~ are generated by means of the random-number generator ~~(80)~~.

5. **(Currently Amended)** **The integrated circuit according to claim 1, wherein** ~~**The integrated circuit (1) as claimed in claim 1, characterized in that**~~ function modules ~~(2)~~ comprise a real-time clock ~~(8)~~.

6. **(Currently Amended)** **The integrated circuit according to claim 1, wherein** ~~**The integrated circuit (1) as claimed in claim 1, characterized in that**~~ operating parameters ~~(f, T, U)~~ to be monitored additionally is the clock frequency ~~(f)~~ of the real-time clock ~~(8)~~ and/or an operating temperature ~~(T)~~ at a point in the integrated circuit ~~(1)~~ and/or an operating voltage ~~(U)~~ of the integrated circuit ~~(1)~~.

7. **(Currently Amended)** **The integrated circuit according to claim 1, wherein** ~~**The integrated circuit (1) as claimed in claim 1, characterized in that**~~ at least one limit value is predetermined for the operating parameter ~~(f, T, U)~~ to be monitored, the operating parameter ~~(f, T, U)~~ is measured and compared with the limit value and when the result exceeds or

drops below the limit value, the content of the first memory is deleted.

8. **(Currently Amended)** **The integrated circuit according to claim 1, wherein** ~~**The integrated circuit (1) as claimed in claim 1, characterized in that**~~ it is arranged in a package ~~**(30)**~~ and has terminal contacts ~~**(31)**~~ brought out of the package ~~**(30)**~~.

9. **(Currently Amended)** **The integrated circuit according to claim 1, wherein** ~~**The integrated circuit (1) as claimed in claim 1, characterized in that**~~ individual function modules ~~**(2)**~~ have an essentially planar extent and are arranged adjacently to one another in the area of the normal to the surface.

10. **(Currently Amended)** **The integrated circuit according to claim 1, wherein** ~~**The integrated circuit (1) as claimed in claim 1, characterized in that**~~ the function modules ~~**(2)**~~ comprise an integrated voltage regulator which regulates an operating voltage ~~**(U)**~~.

11. **(Currently Amended)** **The integrated circuit according to claim 1, wherein** ~~**The integrated circuit (1) as claimed in claim 1, characterized in that**~~ it is constructed as semiconductor chip ~~**(13)**~~.

12. **(Currently Amended)** **The integrated circuit according to claim 11, wherein** ~~**The integrated circuit (1) as claimed in claim 11, characterized in that**~~ semiconductor structures of the

individual function modules ~~(2)~~ are intermeshed in the manner of a puzzle in order to avoid individual function modules ~~(2)~~ from being recognizable.

13. **(Currently Amended)** **The integrated circuit according to claim 11, wherein** ~~**The integrated circuit (1) as claimed in claim 11, characterized in that**~~ an active protective layer ~~(20)~~ which consists of at least one elongated electrical line ~~(21)~~ which extends along the surface of the die, particularly in mutually parallel tracks section by section, is applied directly to the die of the semiconductor chip ~~(13)~~.

14. **(Currently Amended)** An arrangement comprising an integrated circuit ~~(1)~~ as claimed ~~**in one of claims 1 to 13**~~**claim 1**, ~~**characterized in that**~~**wherein** the integrated circuit ~~(1)~~ is connected by means of a data bus ~~(32)~~ to a second memory ~~(40) [RAM]~~ in which data are stored encrypted, wherein the second memory ~~(40)~~ has memory cells which in each case have a memory address and each memory cell can be addressed directly in reading or writing manner.

15. **(Currently Amended)** The arrangement comprising an integrated circuit ~~(1)~~ as claimed ~~**in one of claims 1 to 13**~~**claim 14**, ~~**characterized in that**~~ **wherein** the second memory ~~(40)~~ is volatile and is connected to a battery ~~(43)~~ so that the voltage supply is maintained when another power supply is lacking.

16. **(Currently Amended)** **The arrangement comprising an integrated circuit as claimed claim 1, wherein** ~~**The arrangement comprising an integrated circuit (1) as claimed in one of claims 1 to 13, characterized in that**~~ the integrated circuit ~~**(1)**~~ is connected by means of a data bus ~~**(32)**~~ to a non-volatile third memory ~~**(41), particularly a flash memory or ROM,**~~ in which data or program code are stored encrypted.

17. **(Currently Amended)** The arrangement comprising an integrated circuit ~~**(1) as claimed in**~~ **according to** claim 1, ~~**characterized in that**~~**wherein** the security sensor system ~~**(9)**~~ is connected to a battery ~~**(43)**~~ so that the voltage supply is maintained if another power supply is lacking.

18. **(Currently Amended)** The arrangement comprising an integrated circuit ~~**(1) as claimed in**~~ **according to** claim 1, ~~**characterized in that**~~ **wherein** the security sensor system ~~**(9)**~~ is connected to an auxiliary power source ~~**(12)**~~, integrated in the package ~~**(30)**~~, which provides the power for deleting the first memory ~~**(7)**~~.

19. **(NEW)** The arrangement comprising an integrated circuit as claimed claim 16, wherein the third memory is a Flash memory or ROM.

20. **(NEW)** An integrated circuit comprising function modules, wherein the function modules comprise a central processing unit designed to process data and to execute programs, and a cache memory, wherein the function modules comprise an encryption unit designed to encrypt and decrypt data and the function modules comprise a security sensor system by means of which at least one operating parameter of the integrated circuit is monitored, wherein, as operating parameters, the state of a protective layer on the integrated circuit is monitored, wherein the function modules comprise a random-number generator and a first memory in which cryptological keys are stored, and wherein cryptological keys which are stored in the first memory are generated by means of the random-number generator.